Daniel Hiranandani

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RESUME

Education:

University of California, Santa Cruz, September 2009 to June 2012
Master's of Computer Engineering, Emphasis in Computer Networks, GPA: 3.80

California Polytechnic State University, San Luis Obispo, September 2004 to June 2009
Bachelor's of Computer Engineering, GPA: 3.47

Work Experience:

Google Platforms Networking Software Engineer June 2012 – Current
- Lots of large-scale networks.

Google Platforms Networking Software Engineering Intern June 2011 – September 2011
- Ported network stack to evaluation hardware with new vendor switch chip
- Worked with Google hardware and software engineers, as well as vendor's field application engineers

Teaching Assistant at University of California, Santa Cruz
- Computer Systems and Assembly Language (CMPE 012) Winter 2012
- Intro. to Networking and the Internet (CMPE 80N) Winter, Spring, Fall 2011
- Personal Computer Concepts (CMPE 003) Fall 2009 through Fall 2010

Duties:
- Created cheating-detection software in VBA for Microsoft Office files
- Held lecture/lab sections, graded assignments, prevented mental breakdowns via email, proctored exams, responsible for 50-200 students per quarter

iControl Networks Software Engineering Intern June 2010 – September 2010
- Lead research and analysis of 802.11n repeater performance and reliability tests
- Independently designed and developed for Atmel-based LED controller
- Implemented Real-Time Clock (RTC), I2C, and SPI drivers on Atmel-based devices
- Assisted in schematic reviews and hardware testing/bringup for several devices

Raytheon Space and Airborne Systems Soft. Eng. Intern June 2009 – September 2009
- Designed and developed dynamic Command Input and Display Tool with VBA, Perl, and XML, used for Radar hardware testing and analysis of output data
- Obtained United States Department of Defense Secret Clearance

AeroVironment Software Engineering Intern June 2008 – September 2008
- Created software to control/monitor Broadcom chip on in-house network switches
- Worked extensively with Microchip's TCP/IP Stack
- Developed for Motorola ColdFire and Microchip PIC18 processors

Skills:

- Proficient in C, VBA, Perl, and Assembly (MIPS and Motorola)
- Experience in Shell scripts, C++, Matlab, Java, Python, and PHP
- Firmware for Microchip PIC, Atmel ATxMega, and Motorola 8-bit microcontrollers
- Designing, implementing, analyzing, and simulating (NS-2) network protocols
- Proficient in using an oscilloscope, logic analyzer, multimeter, and a debugger to solve digital and analog issues caused by software and hardware

Projects:

- Cal Poly Senior Project was remote device tracking using SMS and Google Maps. Involved interfacing a GPS receiver and cell phone to a development board with an LCD, an embedded web server running Microchip's TCP/IP Stack serving a dynamic Google Maps page, and communication between the development board and server through SMS messages
- Computer System Design class interfaced Motorola M68HC12 with external ROM, RAM, UART, graphic LCD, LEDs and buttons via parallel bus to create Pong in Assembly
- Programmable Logic Devices class at Cal Poly (CPE329) involved using MicroBlaze soft-core processor on top of Xilinx development board using EDK

Research:

Standards, Metrics, and Benchmarks in MANETs September 2010 – June 2012

- Currently researching metrics and scenario candidates for standardizing evaluations of Mobile Ad-Hoc Network (MANET) routing protocols

Epidemic Routing in Disruption Tolerant Networks January 2010 – June 2010

- Added "Immunization Vectors" to Epidemic protocol to reduce network overhead while maintaining high delivery ratio

International Computer Engineering Experience (ICEX) January 2009 – March 2009

- Created sonar maps of ancient underground water cisterns on island of Malta using Simultaneous Localization and Mapping (SLAM) algorithm and VideoRay ROV
- Developed parser to extract and interpolate GPS data from Smart Tether used to enhance accuracy of sonar maps
- Designed and implemented nonlinear joystick controls for the ROV

Selected Publications:

The Malta Cistern Mapping Project: Underwater Robot Mapping and Localization within Ancient Tunnel Systems, White, C., Hiranandani, D., Olstad, C.S, Buhagiar, K., Gambin, T., and Clark, C.M, *Journal of Field Robotics,* July/August, 2010.

Underwater Robots with Sonar and Smart Tether for Underground Cistern Mapping and Exploration, Hiranandani, D., White, C., Clark, C.M, Gambin, T., and Buhagiar, K., *Proc. of VAST International Symposium on Virtual Reality, Archaeology and Cultural Heritage (VAST 09)*, Sep, 2009.

U.S. Patents:

Fault-Tolerant, Frame-Based Communication System, Rolland Mitchell Koch, William Stuart Sechrist, Daniel Bailey Hiranandani, Patent #12,889,284.

Active Multi-Path Network Redundancy with Performance Monitoring, Rolland Mitchell Koch, William Stuart Sechrist, Daniel Bailey Hiranandani, Patent #12,889,293.

Academic Honors And Awards:

Outstanding Teaching Assistant, 2010-2011
College of Engineering Dean's List, Fall 2004, Fall 2007, Spring/Fall 2008, Spring 2009
Clifford & Juliette Sponsel Scholarship May 2005, 2006
National Society of Collegiate Scholars member May 2005
The National Dean's List, 2004-2005

Relevant Classes:

University of California, Santa Cruz

- Database Systems CMPS180, Winter 2011
- Analysis of Algorithms CMPS201, Fall 2010
- Introduction to Analysis of Algorithms CMPS102, Spring 2010
- Wireless and Mobile Networks CMPE257, Winter 2010
- Distributed Systems CMPS232, Winter 2010
- Computer Networks CMPE252A, Fall 2009
- Computer Architecture CMPE202, Fall 2009

California Polytechnic State University, San Luis Obispo

- Advanced Computer Networks CPE465, Spring 2009
- Introduction to Remote Sensing EE424, Spring 2009
- Computer Vision (Matlab and OpenCV), Winter 2009
- Computer Networks CPE464, Fall 2008
- Computer System Design (M68HC12) CPE439, Spring 2008
- Operating Systems CPE453, Spring 2008
- Mobile Autonomous Robots CPE482, Winter 2008
- Classic Control Systems EE302, Winter 2008
- Systems Programming (C and UNIX) CPE357, Fall 2007
- Analog Signal Processing EE228, Spring 2007
- Programmable Logic Devices (Xilinx EDK) CPE329, Spring 2007
- Digital Electronics and Integrated Circuits EE306, EE307, Fall 2006, Winter 2007
- Computer Architecture CPE315, Summer 2006